UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,063	01/12/2001	Kevin M. Harer	4000/9	2596

35795 7590 11/29/2004

JONATHAN T. KAPLAN
ATTORNEY AT LAW
140 NASSAU STREET
NEW YORK, NY 10038-1501

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,063	HARER ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 were examined.

SECTION I

Response to Applicants' Arguments

Abstract

2. Applicants are thanked for addressing this issue. Objection is withdrawn.

Trademarks

3. Applicants are thanked for addressing this issue. Objection is withdrawn.

Appendix

4. Applicants are thanked for addressing this issue. Examiner and applicants are in agreement as per the telephone interview.

Information Disclosure Statement

5. Applicants are thanked for addressing this issue; however, since the applicant chose not to respond, the objection stands.

Claim Interpretation

6. The applicant can disregard the statements from the examiner.

35 USC § 101

7. The examiner withdraws the negative connotation of the word "useful" in the first office action. The claims appear to be a recurring set of sequences with no post-solution or final result. The only post-solution event appears to be the "monitoring" segment (e.g. claim 9), which is not internal to the device but rather an outside agency (i.e., the analyst). Furthermore, the applicants have not provided any factual evidence to refute examiner's rejection; therefore the rejection stands.

35 USC § 112.

8. Applicants' are thanked for addressing this issue, which is acknowledged and accepted by the examiner. Rejections 112 1st and 2nd are withdrawn.

35 USC § 102

9. Applicants' are thanked for addressing this issue. Although the prior art's publication date is less than one year, its publication discloses a *plurality of inventors.* The 35 USC § 102(a) rejection was documented into the prosecution because ownership of the invention was unspecified. See *In re Katz* 214 USPQ 18.35

USC § 103

10. Applicants' are thanked for addressing this issue. Since part of the prior art used in the 102(a) rejection stands for the latter reasons, the 103 rejection stands.

SECTION II

Objections

11. Claim 25 recites the limitation of a computer usable medium comprising but later discloses computer readable program. There is insufficient antecedent basis for this limitation in the claim.

Rejections

12. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

13. Claims 17-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to using two types of simulation microprocessors. The claims are not tangible because they appear to recite a mathematical algorithm, as admitted by applicants ("Smart Simulation using Collaborative Formal and Simulation Engines" pg. 123, left column 2nd paragraph), which reflects no internal post solution activity.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

15. Claims 1-5, 9-13,17-21,25-29 are rejected under 35 U.S.C. 102 (a) as being anticipated by Ho et al. ("Smart Simulation Using Collaborative Formal and Simulation Engines"; IEEE (November 2000)).

Ho et al. teaches a simulation-based functional verification tool which provides automatic test generation and unreachability analysis (abstract: lines 1-5).

Claim 1: A method of verifying a design for a microcircuit (pg. 120, left column, 3rd paragraph) the method comprising: beginning random simulation (pg. 120, right paragraph, lines 4-13) of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model to obtain a sequence of random simulation states; monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation (pg. 122, left column, lines 1-7) of a sequence of states of said microcircuit design; beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation (pg. 122, left column, second paragraph) states in a formal simulation model of said microcircuit design; monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit

design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 2: The method of Claim 1, wherein said random simulation model and said formal simulation model are the same (pg.121, right column, 6th paragraph).

Claim 3:The method of Claim 1, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 1-16).

Claim 4: The method of Claim 1, wherein said simulating a sequence of formal simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 5: The method of Claim 1, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 9: A method of verifying a design for a microcircuit (pg. 12, left column, 3rd paragraph), the method performed by a data processing system and comprising: beginning random simulation (pg. 120, right paragraph, lines 4-13) of a sequence of

states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model to obtain a sequence of random simulation states; monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation of a sequence of states of said microcircuit design; beginning formal simulation (pg. 122, left column, lines 1-7) of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states (pg. 122, left column, second paragraph) in a formal simulation model of said microcircuit design; monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design (pg. 123, left column, 3rd paragraph, lines 13-19); and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model (pg. 123, left column, 3rd paragraph, lines 13-19).

Claim 10: The method of Claim 9, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 11: The method of Claim 9, wherein said simulating a sequence of formal simulation 10 states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 1-16).

Claim 12: The method of Claim 9, wherein said simulating a sequence of formal simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 13: The method of Claim 9, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 17: A data processing system for verifying a design for a microcircuit, the system comprising (pg. 124, right column, 3rd paragraph): a circuit configured for random simulation of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model (pg.120, right paragraph, lines 4-13) to obtain a sequence of random simulation states; a circuit configured for monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation of a sequence of states of said microcircuit design; a circuit configured for beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states (pg. 122, left column, second paragraph) in a formal simulation model of said microcircuit design; a circuit configured for monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of

states of said microcircuit design (pg. 123, left column, 3rd paragraph, lines 13-19); and a circuit configured for resuming said generation of said random input vector sequence for said random simulation mode' of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 18: The system of Claim 17, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 19: The system of Claim 17, wherein said simulating a sequence of formal simulation 15 states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 1-16).

Claim 20: The system of Claim 17, wherein said simulating a sequence of formal simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 21: The system of Claim 17, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 25: A computer program product comprising a computer usable medium having computer readable code embodied therein for verifying a design for a microcircuit, the computer program product comprising (pg. 120, right column, first paragraph): computer readable program code devices configured to cause a computer to effect random simulation of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model to obtain a sequence of random simulation states; computer readable program code devices configured to cause a computer to effect monitoring of a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation (pg. 120, right paragraph, lines 4-13) of a sequence of states of said microcircuit design; computer readable program code devices configured to cause a computer to effect beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states in a formal simulation model of said microcircuit design; computer readable program code devices configured to cause a computer to effect monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design (pg. 123, left column, paragraphs 2 through 3); and computer readable program code devices configured to cause a computer to effect resuming (pg. 124, right column, section 4, 1st paragraph) said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating

of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 26: The product of Claim 25, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 27: The product of Claim 25, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 28: The product of Claim 25, wherein said simulating a sequence of formal simulation 10 states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 29: The product of Claim 25, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim Rejections - 35 USC § 103

16. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

17. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 6-8, 14-16, 22-24,30-36 are rejected under 35 U.S.C. 103 (a) as unpatentable by Ho et al. ("Smart Simulation Using Collaborative Formal and Simulation Engines"; IEEE (November 2000)) in view of Harer ("Design and Maintenance Specification for CTG Reachability & Control Subsystems" February 2000).

Ho et al. teaches a simulation-based functional verification tool which provides automatic test generation and unreachability analysis (abstract: lines 1-5); but doesn't teach injecting a previously simulated process or input vector.

Harer teaches injecting a previously completed simulation process to obtain the best possible outcome for a predetermine goal.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use Harer to modify Ho since it would be advantageous to rid the chip/microprocessor of all possible errors to negate product recalls to avoid decreases in profits.

Claim 6: The method of Claim 1, wherein said beginning of formal simulation is initiated by simulating in said formal simulation model (Ho: pg. 122, left column, 2nd paragraph, lines 1-4) a state of said microcircuit design previously simulated by inputting at least a portion of said random input vector sequence to said random simulation model (Harer: pg. 9,instructions 4 and 5).

Claim 7: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4), further comprising proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg 9, instruction 8).

Claim 8: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4), wherein said process of monitoring said simulation coverage progress metric, beginning formal simulation, monitoring said formal coverage progress metric (Ho: pg. 122, left column, 2nd paragraph, lines 1-4), and resuming said random simulation is continued

until a previously defined set of goal states of said microcircuit design are simulated or proved not reachable (Harer: pg. 9, instructions 7-10).

Claim 14: The method of Claim 9, wherein said beginning of formal simulation (Ho: pg. 122, left column, 2nd paragraph) is initiated by simulated by inputting at least a portion of said random input vector sequence to said random simulation model (Harer: pg. 9, instruction 5).

Claim 15: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), further comprising proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg. 9, instructions 6 and 7).

Claim 16: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), wherein said process of monitoring said simulation coverage progress metric, beginning formal simulation, monitoring said formal coverage progress metric, and resuming said random simulation is continued until a previously defined set of goal states of said microcircuit design are simulated or proved not reachable (Harer: pg. 9, instructions 6-8).

Claim 22: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), wherein said beginning of formal simulation is initiated by simulating in said formal simulation model a state of said microcircuit design previously simulated by inputting at least a

portion of said random input vector sequence to said random simulation model (Harer: pg. 9, instruction 4).

Claim 23: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), further comprising a circuit configured for proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg 9, instruction 8).

Claim 24: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), wherein said circuits are configured such that said process of monitoring said simulation coverage progress metric, beginning formal simulation, monitoring said formal coverage progress metric (Ho: pg. 122, left column, 2nd paragraph, lines 1-4), and resuming said random simulation is continued until a previously-defined set of goal states of said microcircuit design are simulated or proved not reachable (Harer: pg. 9, instructions 7-10).

Claim 30: The product of Claim 25 (Hop. 120, right column, first paragraph), wherein said beginning of formal simulation is initiated by simulating in said formal simulation model a state of said microcircuit design previously simulated by inputting at least a portion of said random input vector sequence to said random simulation model (Harer: pg. 9, instructions 6 and 7).

Claim 31: The product of Claim 25 (Ho: pg. 120, right column, first paragraph), further comprising proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg. 9, instructions 6-8).

Claim 32: The product of Claim 25 (Ho: pg. 120, right column, first paragraph), wherein said process of monitoring said simulation coverage progress metric, beginning formal simulation, monitoring said formal coverage progress metric, and resuming said random simulation is continued until a previously defined set of goal states of said microcircuit design are simulated or proved unreachable (Harer: pg. 9, instructions 7-12).

Claim 33: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state (Harer: pg. 8, instructions 1-3); and resuming said generation of said random input vector sequence for said random simulation model (Harer: pg. 123, left column, 3rd paragraph, lines 13-19) of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state.

Claim 34: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), wherein said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state (Harer: pg. 8, instructions 1-3); and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design arid said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state.

Claim 35: The system of Claim 17(Ho: pg. 12, left column, 3rd paragraph), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state (Harer: pg 8-9, instructions 1-12).

Claim 36: The product of Claim 25 (Ho: pg. 12, left column, 3rd paragraph), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start

state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state (Harer: pg 8-9, instructions 1-12).

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is (571) 271-

0365, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (571) 272-3716. The fax number for the group is 703-308-1396.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (571) 272-1400

November 19, 2004

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER